

# THE UOSAT-D PACKET COMMUNICATIONS EXPERIMENT

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## ABSTRACT

This paper describes the Packet Communications Experiment (PCE), which will be the primary payload on the **UoSAT-D** satellite. **UoSAT-D** is to be launched in 1989, along with several other Amateur PACSATs. The PCE design will be based on results of the UoSAT-OSCAR-11 Digital Communications Experiment, using an **80C186**, 512 kbytes program RAM and 4 Mbytes message-storage RAM. It will be an open-access Amateur Radio PACSAT messaging system.

## INTRODUCTION

Before the end of 1989, Amateur Radio will be able to boast five new packet radio satellites. The launch of an Ariane 40 rocket with the French SPOT-2 imaging satellite as primary payload will mark an unprecedented expansion in the number of Amateur Radio satellites in orbit. Six secondary payloads will be launched beneath SPOT-2: 4 Microsats built by **AMSAT-NA** and its collaborators, and 2 **UoSATs** built at the University of Surrey. At least five of these satellites will have AX.25 packet radio data links, and several will be dedicated 'PACSATS' for store-and-forward packet radio message handling.

One of the new PACSATs will be **UoSAT-D**, carrying a Packet Communications Experiment (PCE) as its primary payload. The PCE is based on an **80C186** processor with 512 kbytes of program RAM and a **4-Mbyte RAMDISK** for message storage. 9600 **bits/sec** FSK packet links will make this the fastest of the new PACSATs. The PCE will implement the AX.25 link protocol in support of a range of higher-level protocol experiments. The **UoSAT-D** PCE, described in this paper, will be an open-access PACSAT transponder for Amateur Radio stations.

## 1.0 RESULTS FROM THE UOSAT-OSCAR-11 DCE

Previous experiences with store-and-forward satellite operation have influenced the PCE design. In particular, the UoSAT-OSCAR-11 Digital Communications Experiment or DCE has provided valuable data (Ref. **1, 2, 3**). The DCE, built by **AMSAT** volunteers in the USA and Canada, was included on UO- 11 to provide in-orbit tests of radiation effects on VLSI components and to prove that store-and-forward communications using low-cost satellites and small earth terminals was possible. The DCE has been a great success, providing unique engineering data, forwarding amateur packet messages internationally, and saving UoSAT-OSCAR-11 from a failed on-board data link.

The DCE hardware is an NSC-800 microprocessor, an **82C55** parallel I/O chip, and memories ranging in density from **4k X 1** bit to **8k X 8** bit. With exceptions detailed in Ref. 3, these devices have survived the radiation dose of 4 years in a **700** km polar orbit.

### 1.1 Radiation-Induced Single Event Upsets

One of the most interesting aspects of the DCE mission has been the monitoring of cosmic particle induced bit-flips or single event upsets (**SEUs**) in CMOS static memory. **SEUs** in the memory protected by hardware error detection and correction (EDAC) and in the unprotected memory are monitored by DCE software.

In 144 kbits of EDAC-protected memory - composed of 4k X 1-bit devices - 60 SEUs have been recorded in the last two years. The mean error rate estimate is:

$5.98 \times 10^{-7}$  errors/bit/day. [See Note 1]

In practical terms, this error rate means that you can expect your software to crash once per day if you have 240 kbytes of this memory with no EDAC hardware. The DCE's EDAC hardware has protected it from any such crashes.

SEU monitoring on the 8-bit wide memories began in earnest during 1988. This memory is allocated in 256-byte blocks for message storage. Each block is divided into two 128-byte 'words', each of which is protected by a 3-byte EDAC code. This code is two 8-bit CRCs and an exclusive OR sum. The CRCs (generated by table lookup for speed) locate errors, while the checksum gives the error pattern. This EDAC code can locate and correct any byte-wide error in a 128-byte word. Memory wash software periodically checks each word for errors, logging and correcting any which are found. Twenty one errors were found over the 48 days that this software has been fully operational. This implies an error rate of:

$5.70 \times 10^{-7}$  errors/bit/day.

This is strikingly similar to the rate for the bit-wide memories, indicating that the bit-wides and the denser byte-wides have approximately the same SEU sensitivity - contrary to what we might intuitively expect. SEU susceptibility is related to feature size and device geometry, and UoSAT is undertaking a collaborative research project with the European Space Agency (ESA-ESTEC) to use the UoSAT-2 SEU measurements in refining ground-based SEU models and component tests.

All of the errors observed in byte-wide memories have been single bit errors, and this significant observation has influenced the UoSAT-D PCE design. Previously, we thought that the dense packing of bits in byte-wide devices would mean that one cosmic particle might upset several bits in a single byte. Since multi-bit errors are not corrected by the hardware EDAC circuits (based on the Hamming (8,12) code), byte-wide memories were never used for spacecraft EDAC memory. The in-orbit observations of the DCE show that multi-bit errors are not common in byte-wide devices, implying that byte-wide devices can be used in EDAC memory for storing programs and critical data.

## 1.2 Message Forwarding Experiments

While acting as a hardware test-bed, the DCE has also been used as a communications channel, linking Amateur Radio packet networks in the U.K., Australia, New Zealand and South Africa through BBS mail forwarding. A total of 10 gateway groundstations (including one in Antarctica and two in Pakistan) have been activated during the experiment, and 6 are now passing BBS traffic via UoSAT-2. Although this is a small population, it has provide some insight into the operation of satellite gateways for digital communication.

Three important observations follow:

- The introduction of reliable packet satellites which can be interconnected with the existing BBS networks will make Amateur Radio packet networks truly international. The current mail addressing and routing system breaks down when several international transport systems are available. We must quickly look for solutions to international addressing and routing problems.
- The DCE is data transparent, and it has frequently been used to forward binary files and archived text. Text archiving (using the common PKARC/PKXARC combination) provides compression of up to 60%. This simple procedure can have the combined effect of doubling a link's data throughput and doubling the memory available on the satellite. The packet radio community should adopt a suitable standard for compressed text and use it whenever possible.

**oProtocols** which are **efficient** for terrestrial BBS use are not necessarily best for communications with quickly-moving, low-Earth orbiting (LEO) satellites. The DCE **MSG2 protocol** (developed by Price and Ward) has proven quite efficient for moving groups of BBS messages in a single 'transaction' with the satellite. An important **feature** of this protocol is the ability to continue a 'transaction' on a later pass from the point at which you lose the **satellite**. **UoSAT-D** will be used to experiment with specialised LEO satellite protocols above the AX.25 link layer.

## 2 THE **UoSAT-D** PACKET COMMUNICATIONS EXPERIMENT

The UoSAT Unit intended to fly a packet communications system on the **UoSAT-C** satellite (Ref. 4), which was scheduled for launch by NASA/DELTA in 1988. Unfortunately, this launch and the **UoSAT-C** mission have been postponed. The SPOT-2 opportunity, jointly developed by UoSAT, **AMSAT-NA** and Arianespace, became the best time to launch the PCE. The PCE will be the primary payload on **UoSAT-D**, one of the two UoSAT satellites on the SPOT-2 launch.

**UoSAT-D** will be slightly smaller than other **UoSAT-1, 2 & C** satellites, roughly **345** mm square in cross section and 550 mm tall. The modular satellite structure is composed of stacked 345 X 345 X 28 mm 'module boxes', and the PCE occupies two of these boxes.

The design of an advanced store-and-forward transponder at **UoS** is being funded by a contract from the Volunteers In Technical Assistance (VITA). VITA wish someday to use store-and-forward communications on non-Amateur frequencies to link their headquarters in Washington, DC with technical **volunteers** in remote **rural** areas of developing countries. The PCE hardware flown on **UoSAT-D** will be a prototype for the VITA payloads. Operational experience from the **UoSAT-D** Amateur Radio communications mission will be used to optimise the PCE design, and **final** operational payloads should be ready for a dedicated VITA satellite which could be launched within the next few years.

**AMSAT-UK** is funding a substantial portion **UoSAT-D** mission.

### 2.1 **UoSAT-D** On Board Data Handling

Like **UoSAT-1** and **UoSAT-2**, **UoSAT-D** will carry several on-board computers (**OBCs**) linked in an on-board data handling (OBDH) network. The PCE will act as the primary OBC, backed up by an 1802 similar to those used on **UoSAT-1** and UoSAT- 2. The third OBC is an **80C30** microcontroller dedicated to a radiation monitoring experiment (Cosmic Particle Experiment / Total Dose Experiment - **CPE/TDE**). These **OBCs** will be linked by a multiple access serial bus using 9600 **bit/sec** asynchronous packets. Most of the data on the OBDH bus will be **CPE/TDE** output being sent to the PCE for storage and later packet downlinking.

Telemetry and teiecommand can function as stand-alone hardware systems or as peripherals to the **OBCs**. Telemetry is accessed through parallel links; the OBC generates a channel address and the telemetry system returns a **12-bit** A-to-D converter value. The **OBCs** have serial inputs to the teiecommand system; 1200 **bit/sec** command packets with error detection information are sent to the command decoder, where they are verified, decoded and latched. This system combines the flexibility of computer driven telemetry and teiecommand with the reliability of stand-alone hardware. This combination has proven itself on the previous **UoSATs**, where hardware problems have been circumvented through alternative communications paths, and the missions are frequently enhanced by software upgrades.

## 3. PCE HARDWARE

The PCE is separated into two module boxes. One box contains the CPU, program memory and peripherals, while the second holds a **4-Mbytes RAMDISK** for message storage.

### 3.1 PCE CPU and Memory

The Packet Communications Experiment CPU module (PCE CPU) is an **onboard** computer intended to be the primary operational OBC on **UoSAT-D**. Parallel interfaces for telemetry, magnetometer, battery charge regulator A-to-D converter and **RAMDISK** are provided. Four serial channels serve telecommand, DASH and packet radio channels. (Fig. 1)

The PCE CPU is an **INTEL 80C186** microprocessor running at 7.3728 MHz. This processor, of unknown radiation tolerance, was chosen because it represents the state of the art in highly-integrated CMOS microprocessors (Ref. 5). It provides clock generator, Interrupt controller, DMA controller, timers, chip-select generation and a **16-bit 8086-compatible** CPU in a single package. None of the processors for which we have radiation tolerance data provide this much function in such an efficient package.

The **80C186**, with full **16-bit** bus, was chosen to allow demanding multi-tasking experiments. As the primary OBC on **UoSAT-D**, the PCE will execute the following tasks:

- closed-loop attitude control, using magnetorquing algorithms which will keep the satellite Earth-pointing to within 5 degrees,
- power conversion optimisation,
- data collection and storage for the radiation experiments,
- long-term telemetry surveys,
- experiments in on-board expert systems and satellite autonomy,
- SEU detection and correction.

Of course, PCE will also provide 9600 bit/second packet communications. The high bus bandwidth of the **80C186** is justified in this demanding environment. The word-wide bus requires **more** power and PC board area than the **80x88-style** byte-wide bus, but this was considered a reasonable tradeoff given the size of the **UoSAT-D** PC boards and the power available. The **80C186** is also a more mature product than the **80C188**, and it is available as an extended temperature range device.

The PCE CPU board contains 256 kbytes of EDAC RAM for programs and critical data (e.g. the file allocation tables for the RAMDISK). This EDAC memory will use **32K X 8** chips, since the results of SEU monitoring on the UO-11 DCE indicate that byte-wide memories can be successfully protected by single-bit correcting codes such as the Hamming **(12,8)**. Each **32K** words of EDAC RAM will consist of 4 memory chips, two for the 16 bits of data and one each for the two **4-bit** Hamming check codes. Although consideration has been given to storing the two check codes in one device, this is unduly complicated by the need for **80C186** to make byte-wide writes to memory. Separate error counters will signal errors detected in the high-byte and low-byte memory banks. The EDAC system can be disabled by spacecraft telecommand in case of failure in the detection or correction circuits.

In addition to the EDAC RAM, the PCE CPU will have 256 kbytes of unprotected RAM. Assuming that the SEU rate per bit is similar to that observed on **UoSAT- OSCAR-I 1**, this unprotected memory can be used safely for temporary data storage.

The **RAMs** on the PCE CPU board will be from three different manufacturers, in three different package types. 128 kbytes of EDAC RAM will be standard **.6-inch** wide DIPs, and the other 128 kbytes will be **.3-inch 'skinny-DIPs'**. The non- EDAC RAM will be two Hybrid Memory Systems hybrids, each made with four surface mounted 32k X 8 chips on a single carrier. This mixture provides reliability through dissimilar redundancy.

## 3.2 Input/Output

### 3.2.1 Serial Channels

The **85C30** serial communications controller (SCC) was selected for the PCE because it supports both synchronous and asynchronous serial communications, it has an integral baud-rate generator, and it is well understood by **AMSAT** programmers. The **80C30**, although a faster and more easily programmed device, was not available as an extended temperature-range part at the time the PCE was designed. There are two **SCCs** providing a total of 4 serial channels for packet radio and OBDH.

The PCE requires a flexible serial system, in which either SCC can be used for any of the possible communications tasks. Reliability is inversely proportional to complexity, however, so a comprehensive array of digital selector chips is not used. One channel on each SCC has a digital selector on its input, and the other channels are directly wired to data sources. This system is a compromise between complexity and flexibility.

The downlink HDLC channels are the most sensitive to service timing - too much interrupt latency on these channels will cause transmitted frames to be aborted. Thus, either of the **80C186** DMA channels can be used as an HDLC output channel. The other DMA channel can be switched between HDLC receiving or **RAMDISK** data transfer.

The telecommand interface is a 1200 **bit/sec.** asynchronous serial channel using 8 data bits and an parity bit. For reliability, the telecommand channel is directly connected to the data output of one of the **SCCs**.

The fourth SCC channel is connected to the shared serial OBDH network. This channel will normally handle data packet bursts at 9600 **bits/sec.** If any of the PCE data links fail, however, the OBDH network connection can be used as a link to almost all data-generating and receiving devices on the satellite - particularly to the receivers and transmitters.

### 3.2.2 Parallel Links

The parallel i/O system uses 3 Harris **82C55 PPIs**. The **82C55** in the DCE is still functioning, giving us some confidence in this chip. The nine **8-bit** parallel ports provided by these chips are used for the telemetry system, the **RAMDISK** interface, the navigation magnetometer, and the BCR D-to-A converter.

The DAC deserves further comment. it is a current-output DAC (AD7524) driving a variable set-point input on the battery charge regulator (BCR). The optimum operating point for the BCR is influenced by battery charge state, temperature and solar panel illumination. The PCE will measure this point every five minutes by varying the DAC value and using the telemetry system to watch the solar-panel power output. The DAC value will then be set at the optimum point until the next measurement is made.

The remaining parallel **I/O** bits are used for EDAC counters, digital selector control and **downlink** keying.

## 3.3 The RAMDISK

An operational store-and-forward transponder must provide several megabytes of memory for message storage. SYSOP chores will become onerous and reliability will suffer if too little memory is provided. There are several methods of providing expanded memory within the limited physical address space of the selected microprocessor. In the **UoSAT-OSCAR-11** DCE, bank switching is used, with four banks of memory selected by a parallel port to appear at the top of the processor memory map. The 1802 OBC on UoSAT-OSCAR-11 uses the 192 kbytes of RAM in the Data Store and Readout (DSR) as a sequential memory through a 1200 **bit/sec** serial link. The **UoSAT-D** PCE will use a parallel link between the **80C186** CPU and a **4-Mbyte RAMDISK** module. Although memory-mapped, bank switched mass storage was originally proposed for the PCE, this posed power consumption and redundancy problems. If the 4 Mbytes were in the address space of the processor, they would have to be organised as a **16-bit** wide memory resulting in increased power

consumption and PC board area. A dedicated memory would also be [difficult to share between two processors, ruling out the possible inclusion of a backup processor. So, a **RAMDISK** with parallel interface was chosen.

The **RAMDISK** is divided into individually addressable sectors of 256 bytes each, and the interface is similar to that used by a disk drive. To store data in a sector, the PCE CPU uses control lines to command the **RAMDISK** into write mode, sends two bytes of sector address, and then sends the data. To read a sector, the PCE CPU commands the **RAMDISK** into read mode, sends the sector address and then reads the desired data bytes. Contiguous sectors can be read or written without re-addressing the **RAMDISK**. A bidirectional parallel bus with handshaking and control lines connects the **RAMDISK** and the PCE CPU. If a second microprocessor were available, the **RAMDISK** bus could pass through a digital selector controlled by spacecraft telecommand.

In a 4 Mbyte memory system, it is possible that cosmic particles will cause CMOS **latchup**, or that something (e.g. a failed by-pass capacitor) will result in undesirable power consumption in part of memory. To keep a single failure such as this from disabling the entire system, the memory is divided into four units. Each unit is provided with its own power supply, so that each can be powered down if it fails or is not needed. Each unit is also buffered from the common address bus. One Mbyte of memory will be 128-kbyte hybrids as used in the CPU RAM, the remaining memory will use 256-kbyte SIL hybrids. The control circuits for the **RAMDISK** are implemented in HCMOS, designed for full-speed (1 Mbyte/sec) DMA access by the PCE CPU.

#### 4.0 RF DATA LINKS

UoSAT-D will use FSK uplinks and downlinks as proposed in Ref. 4, but using a Mode-J (70-cm downlink / 2-m uplink) bandplan. Mode-J was chosen after considerable experience with UoSAT-2 showed 70-cm to be significantly quieter at the groundstation than 2 meters. UoSAT-D is designed to provide good downlink data ( $2.5 \times 10^{-5}$  BER) to stations with modest antennas. This requires several dB groundstation antenna gain between 0 and 30 degrees elevation and decreasing gain as the satellite rises and range decreases. This pattern can be achieved by several simple, non-steered antennas. There will be a high-power downlink on the satellite for experiments with very small groundstations and a low power downlink for periods of poor power budget.

Data will be scrambled (to remove DC component) using the same polynomial as the K9NG/TAPR modem. This polynomial is also available on the G3RUH FSK modem.

A Mode-J frequency plan brings with it the problem of identifying uplink channels in the crowded 2-meter band. UoSAT-D and the Microsats will often be visible simultaneously, aggravating this frequency allocation problem. We expand the problem yet again if we use a simple cure for the inefficiency of ALOHA access: four uplinks for each satellite. UoSAT-D will use only one uplink, and it will not have ALOHA access. Possible access techniques are discussed in an accompanying paper "Alternatives to ALOHA for PACSAT Access."

#### 5.0 SOFTWARE

One of the reasons for deciding on the 80C186 CPU was the ready availability of software. The basic multitasking kernel is being supplied by Quadron Services Corporation. The non-mission-specific kernel services are being ported from Quadron's existing multi-tasking system with design input from UoSAT and AMSAT-NA. There is a paper in these proceedings by H Price and B McGwier describing the kernel and the Microsat applications software. UoSAT-D applications programs for packet communications and spacecraft housekeeping will be developed at UoSAT.

## 6.0 CONCLUSION

The simultaneous launch of 5 OSCARS with packet radio capability is an exciting and interesting prospect. **UoSAT-D** will be carrying a PACSAT transponder similar in function to those on the Microsats, yet this transponder will use different hardware, different link speeds and different access techniques. This is an ideal opportunity for experimentation, and it provides in-orbit redundancy never before experienced by **AMSAT**. Once proven in orbit, **80C186** PCE will be a high-performance OBC design for low-Earth orbiting satellites. Through transfer of PCE technology to VITA, Amateur Radio will again have proven itself capable of conducting state-of-the-art research and design with widespread applications.

## ACKNOWLEDGEMENTS

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## NOTES

Note 1: SEU occurrence is assumed to have a Poisson distribution, and the 5% to 95% probability bounds for the measured mean error rates are:

Bit-wide memories (**HM-6564**)                      4. 99X  $10^{-7}$  to 7. 48X  $10^{-7}$

Byte-wide memories (Hitachi 6616 & 6264)                      4. 07 X  $10^{-7}$  to 7. 87 X  $10^{-7}$

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