THE NOISE PERFORMANCE OF SEVERAL DATA DEMODULATORS

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INTRODUCTION

This paper shows the noise performance of several data demodulators currently being used in packet radio. The bit error rate (BER) in presence of white Gaussian noise was measured on the following demodulators:

1) JAS-1 PSK demodulator [1]
2) Discriminator [2]
3) AMD 7910 modem [3]
4) Differential detector [4]
5) G3RUH PSK demodulator [5]
6) EXAR 2211 demodulator [6]

The noise performance of this demodulators is graphically presented here and a brief description of the test gear used in these measurements is given in appendixes A and B.

METHODS

The test setup for the demodulator's performance measurement is shown in figure 1. The V-52 generator produces a pseudo-random test sequence as recommended by the CCITT V-52 standard [7]. Details of this generator are given in appendix A.

The FSK modulator is an EXAR 2206 integrated circuit,

The PSK modulator was specially built for these tests using digital techniques: clock, binary counter, sine look-up table in EPROM and D/A converter. The carrier frequency was set to 1600 Hz and the PSK demodulators were tuned for operation with this frequency,

For both, the FSK and the PSK modulators, an output peak amplitude of 1 volt was chosen. The JAS-1 demodulator was modified to work correctly with this amplitude (the 10-kΩ resistance at the input of U2 was changed to 100-kΩ).

The noise generator was built, as shown in appendix B, filtering a pseudo-random sequence (PN) with a low pass filter [8][9]. This a very simple way to obtain Gaussian noise with a well known power spectral density.

The outputs of the modulator and the noise generator are added by the operational amplifier A1 as shown in figure 1. The output of the noise generator was adjusted to obtain the needed signal to noise ratio. This ratio is defined as:

$$S/N = \frac{Eb}{\eta} = \frac{a^2 \cdot Tb}{2 \cdot \eta} = \frac{a^2}{2 \cdot \eta \cdot Fb} \quad \text{Ec 1}$$

Where Eb is the mean bit energy, η is the one-sided power spectral density of the noise. a is the modulators' output peak amplitud (1 volt), Tb is the bit duration and Fb is the bit rate (1200 bits/s).

The delay shown in figure 1 is another demodulator, identical to that being tested, but this one demodulates the signal in absence of noise and in that way provides a no error data stream with the demodulation delays. The output of this demodulator is also used to recover the bit clock using a state machine [10].

The demodulators' outputs are compared in an exclusive-or gate whose output is a logical "one" only when its inputs are different, i.e. : when there is an error. This errors are sampled by the recuperated bit clock and counted with a standard digital counter.

With this test setup the errors were counted together with the measurement of the duration of the test. At high error rates large error counts are accumulated in a short time, but at low error rates the time interval needed to accumulate even a few errors becomes very large. A large error count is needed to obtain meaningful data, so that it was necessary to adopt the following trade off:

1) Accumulate if possible a large number of errors (N>1000).
2) At low error rates accumulate at least 100 errors,

RESULTS

With the duration of the test and the bit error count, the bit error rate was calculated as:

$$BER = \frac{N}{Fb * T} \quad \text{Ec 2}$$

Where N is the bit error count, Fb is the bit rate (1200 bit/s) and T is the duration of the test.

The bit error rate was plotted versus the signal to noise ratio as shown in figure 2 and the signal to noise ratio needed for a BER = 1E-04 is indicated in table 1.

The JAS-1 demodulator is the best performer and runs very close to the ideal demodulator. This is very important in satellite work using SSB reception where one dB gained at the demodulator is equivalent to one dB gained at the antenna.

It's also interesting to note the poor performance of the most popular packet radio FSK demodulator: the EXAR 2211.

APPENDIX A

The test sequence generator circuit is shown in figure 3. It was built using a 9 stages shift register (IC1 and IC2) whose outputs Q4 and Q8 are added together in a module-two adder (IC3A) and the result is fed back to the first stage, The gates ICY, IC5A and IC5B form the start-up circuit to avoid the "all ceros" sequence. The generator's 1200 Hz clock is built around the Integrated circuits IC6, IC7A and IC7B.

This test sequence generator is a very useful l tool when working with data communication equipment; its bit rate is easily changed choosing the right IC6 output and/or selecting the adecuate crystal resonator.

APPENDIX B

The noise generator is shown in figure 4. The 24 stages PN sequence generator is formed by the shift registers ICI, IC2 and IC3 whose outputs Q0, Q1, Q6 and Q23 are added together in a module-two adder (IC4) and the result is fed back to the first stage. The IC5C, IC5D and IC5E inverters form the start-up circuit to inhibit the "all ceros" sequence, The inverters IC5A and IC5B are part of the 100KHz crystal controlled clock. The operational amplifiers IC6A and IC6B are part of a three pole Butterworth filter with a cut-off frequency of 3400Hz. The output noise level is adjusted with a precision IO turns potentiometer with a digital dial; it is easier and more precise to trust in the potentiometer dial's indication than trying to measure the generator's noise power output. Finally the operational amplifier IC7 buffers the noise output.,

A FN sequence generated with a circuit like the one shown here has a low frequency one-sided power spectral density η given by:

$$\eta = K^2 * \frac{V^2}{2} * \frac{1}{Fc} \quad \text{.....Ec 3}$$

Where K is the reading of the potenciometer's dial ($0 <= K <= 1$), V is the peak to peak amplitude of the PN sequence (in this case the CMOS logic output swings between cero and Vcc, that is V = 15 volts) and Fc is the clock frequency (100KHz). Replacing in Ec 3 we have:

$$\eta = K^2 * \frac{15^2}{2} * \frac{1}{1E+05} =$$

$$= 112.5E\text{-}05 * K^2 [\ V^2/Hz\ ] \quad \text{.....Ec 4}$$

REFERENCES

[1] "A PSK Demodulator for the JAS-1 Satel-1 ite", F. Yamashita, JSIUKR, QEX, August 1986, pp 3-7.

[2] "Optimun Binary FM Reception Using Discriminator Detection and FI Shaping", A.A. Meyerhoff and. W.M. Mazer, RCA Review. December 1961, pp 698-728,

[3] "Am7910 FSK Modern Wor ld-Chip", Advanced Micro Devices data sheet,

[4] "Differential Detection of Binary FM", R.R. Anderson, W.R. Bennet, J.R. Davey and J , Salz, Be l l System Technical Journal, January 1965, pp 111-159.

[5] "JAS-1 Modem", J. Mi l ler, G3RUH, Proceedings of the 4th Annual AMSAT Space Symposium, Dallas, Texas, November 1986, p 148.

[6] "XR2211 Demodulator/Tone Decoder", Exar Integrated Systems data sheet.

[7] 'Characteristics of Distortion and Error-Rate Measuring Apparatus for Data Transmission", International Telegraph and Telephone Consultative Committee (CCITT), Mar del Plata, 1968.

[8] "Shift Register Sequences", S.W. Golomb, Ho lden-Day, Inc., San Francisco, CA, 1967.

[9] "Some Statistical Properties of Smoothed Maximal Length Linear Binary Sequences", P.D. Roberts and R.H. Davies, Proc. 7.E.E, 1966, vol. 113, p 190.

[10] "Xerox Packet Interfase Board", J. Bloom, KE3Z, et al., AMRAD Newsletter, Nov./Dec. 1984.

TRADEMARKS

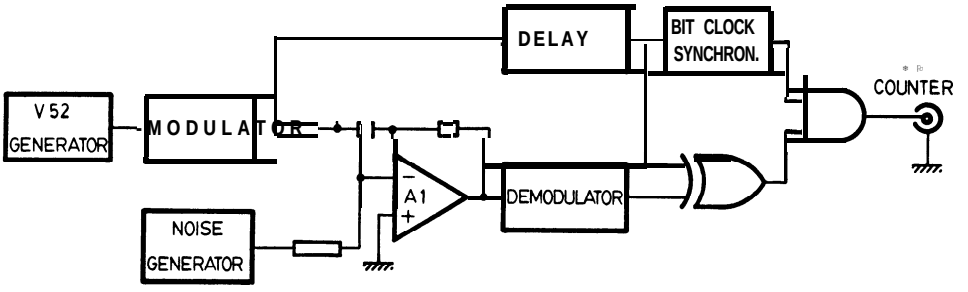


FIGURE 1

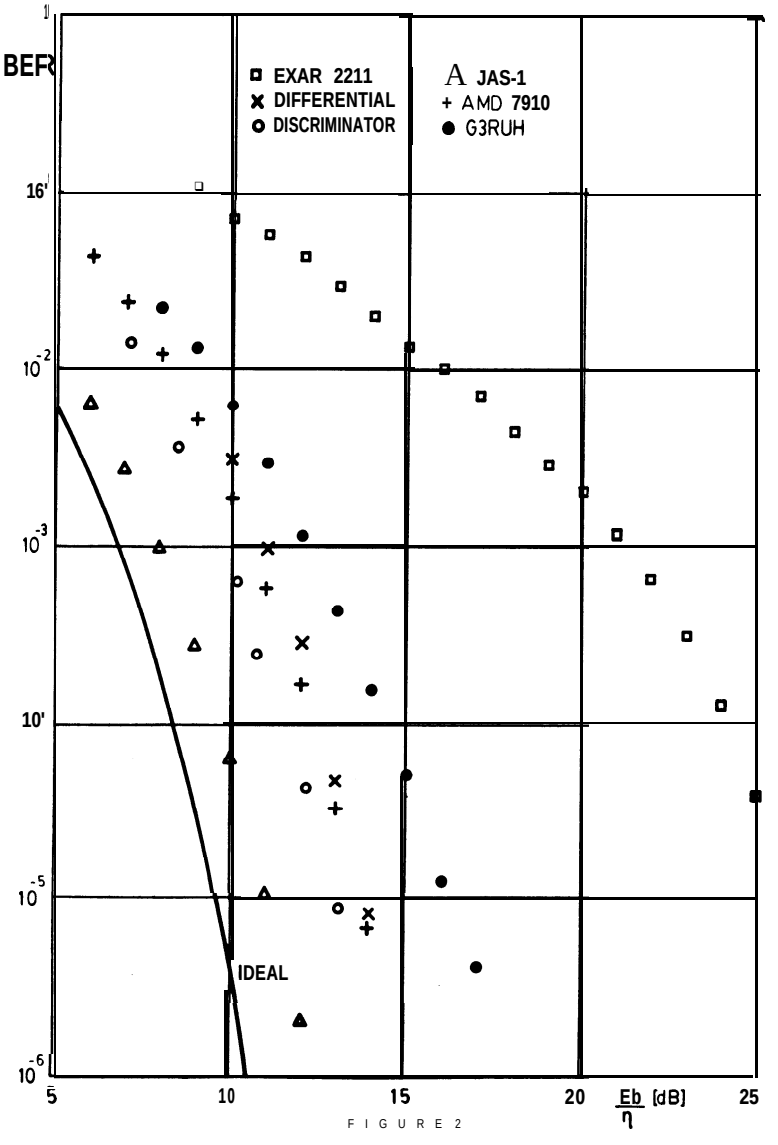


FIGURE 2

DEMODUL.	JAS-1	DISCR.	7910	DIFF.	G3RUH	2211
S/N FOR BER=1E-04	9.7 dB	11.5 dB	12.3 dB	12.6 dB	14.4 dB	24.2 dB

T A B L A No 1

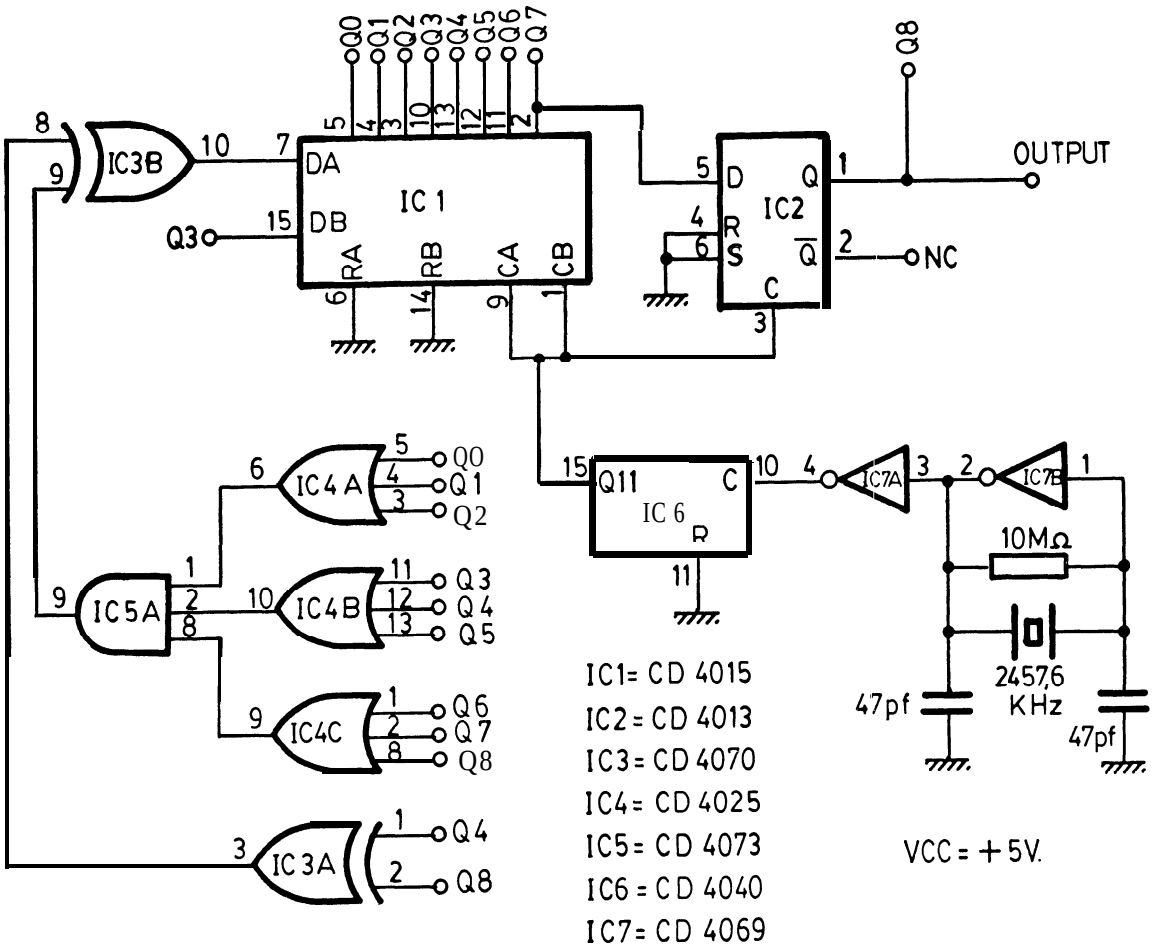
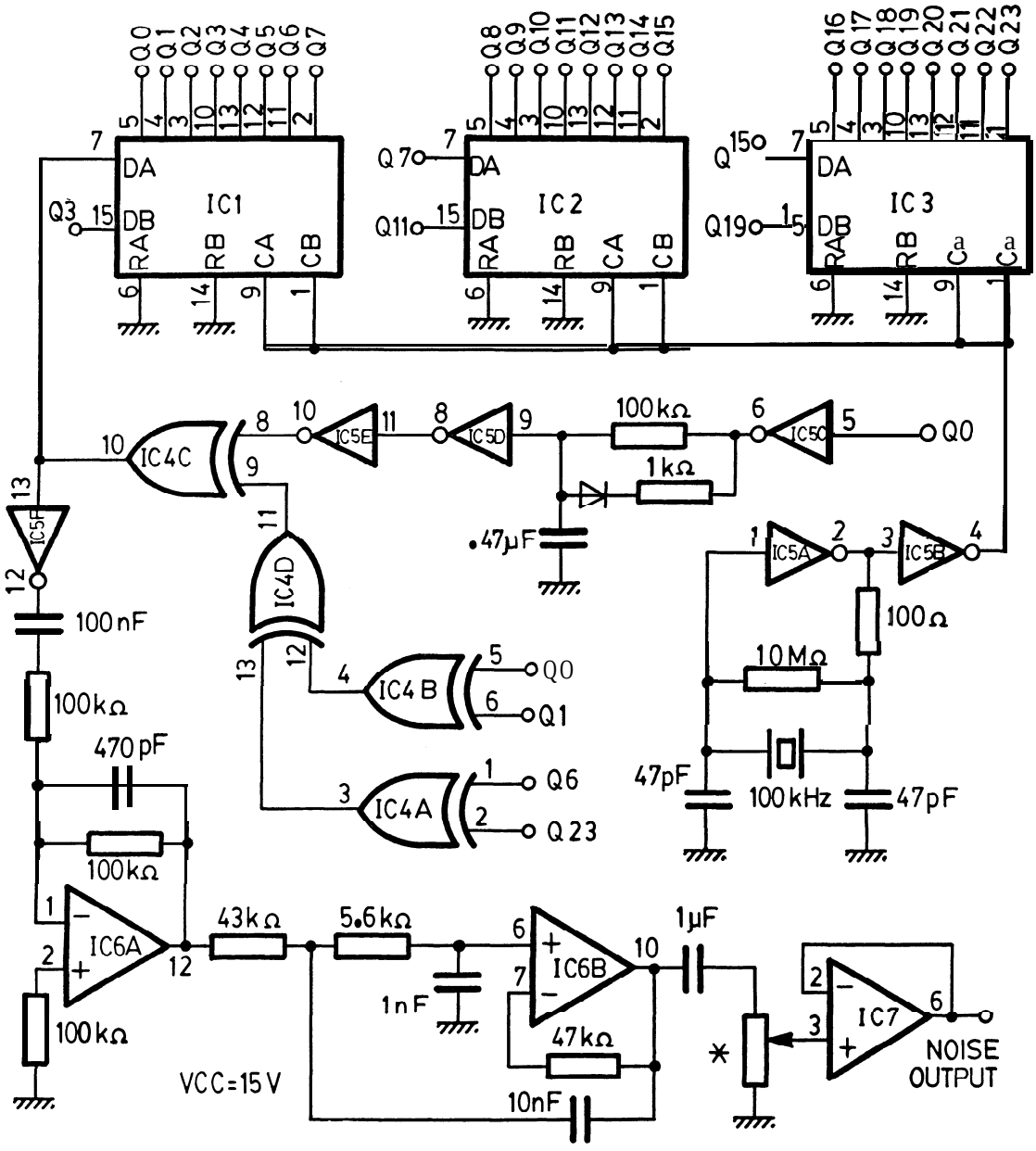


FIGURE 3



IC1-IC2-IC3 = CD 4015
IC4 = CD 4070
IC5 = CD 4069
IC6 = LM 747
IC7 = LM 741

* TRIMPOT 3610-S
10 k OHMS-10 TURN
POTENTIOMETER
WITH DIGITAL DIAL.

FIGURE 4